Amendments to the Drawings:

The attached sheets of drawings include changes to Figs. **1**, **2**, and **4a**. The first sheet, which includes Figs. **1-2**, replaces the original sheet including Figs. **1-2**. In Figs **1-2**, previously omitted parasitic capacitor **Cp** has been added. The second sheet, which includes Figs. **4A-B**, replaces the original sheet including Figs. **4A-B**. In Fig. 4a, the element titled **C parasitic** has its titled shorted to **Cp** to conform with the element added to Figs. **1-2**.

<u>Attachment:</u>

Annotated Sheets Showing Changes

Replacement Sheets

REMARKS/ARGUMENTS

Examiner Nguyen is thanked for the thorough examination of the subject Patent Application. The Claims have been carefully reviewed and amended, and are considered to be in condition for allowance.

Reconsideration of the rejection under 35 USC §112, second paragraph, of Claims 1-11 as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention is requested in light of the following arguments. Claims 1-11 are amended to more clearly define the "large capacitor" that is added between the bias node **b1** and the lower supply voltage **VSS**. The value of the large capacitor **CHC** is chosen such that the capacitance coupling ration between the large capacitor and the parasitic capacitor **Cp** between the bias node **b1** and the lower supply voltage **VSS**, is sufficiently large that the bias voltage **VB11** is directly coupled to the lower supply voltage **VSS**. The PMOS bias node is now the bias node **b1** and appropriately defined.

Claims 3-9 are amended to depend on Claim 2. Claims 10 and 11 are amended to define the coupling of the parasitic capacitor **Cp** between the bias node **b1** and the lower supply voltage **VSS**.

Reconsideration of the rejection under 35 USC §102(e) of Claims 1-11 as being anticipated by U.S. Patent 6,437,613 (Shim et al.) is requested in light of the following arguments.

Shim et al. does provide a first comparator **61** and second comparator **63** having a differential structure similar to the buffer input portion of this invention. However, Shim et al. does not include

> a large capacitor between the bias node and a lower supply voltage said large capacitor providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point approaching a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point; (Claim 1, Lines 4-10)

and

> a buffer output portion in communication with the buffer input portion for producing an output signal. (Claim 1, Lines 11-12)

The transistor **61a** is configured to be turned off and turned on according to the "voltage level of the first auxiliary signal VAUXL." The "voltage level of the first

comparison signal VCOML is prevented from being unstable." (Shim et al. Col. 6, Lines 27-33) The transistor **61a** is not configured as a large capacitor that provides a charge couple of the bias node **b1** to the lower supply voltage **VSS**.

Reconsideration of the objection to Claims 2 and 11 because of informalities is requested. The claims are amended to provide correct description of the elements and function of the elements.

Reconsideration of the objection to the specification because of informalities on pages 4 and 5 is requested. The specification has been amended to incorporate the corrections requested by the examiner and to clarify the structure and function of the input buffer receiver of the invention.

Figs. 1, 2, and 4a have been modified with the changes marked in red on the attached drawings to. Approval of these changes is requested. No new matter has been added. Figs. 1 and 2 are modified to include the parasitic capacitor **Cp** present between the bias node and the lower supply voltage. The permits clarification of the description of the large capacitor **CHC** and it effects on the performance of the input buffer receiver of the invention.

Claims 12-42 are added to more completely claims the subject matter the applicant regards as the invention.

The related art references made of record and not relied upon have been reviewed and it is agreed that they do not suggest the present detailed claimed invention.

Applicant respectfully requests that a timely Notice of Allowance for all claims be issued in this case.

It is requested that should Examiner Nguyen not find that the Claims are now allowable, that the undersigned be called at (845) 452-5863 to overcome any problems preventing allowance.

Respectfully Submitted,
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Attachments:

LOW JITTER INPUT BUFFER WITH SMALL INPUT SIGNAL SWING

Background of the Invention

Field of the Invention

[0001] The present invention generally relates to an interface circuit, and particularly to a low jitter input buffer.

Description of Related Art

[0002] Major design efforts have been directed at circuit design techniques involving input circuits for memory devices. A number of solutions have been proposed.

[0003] U.S. Patent 5,978,310 (Bae et al) describes an input buffer for a DRAM memory device, which removes noise from the row address strobe. The device has a data output enable, which can be delayed for a predetermined time, and which also produces a contr o! signal for the output. There is also a buffer output for producing the noise free input according to the control signal.

[0004] U.S. Patent 6,002,618 (Komarek et al) discloses an NMOS input receiver circuit for a read only memory. It includes a feedback loop to control hysteresis. There is a second stage and an additional output for the receiver. Switching noise from inside the memory is isolated and cannot be fed back into the receiver circuit to affect the TTL voltage levels. Wide, long FET sizes are used to minimize manufacture variations in the receiver switching levels.

[0005] What is still needed is a mechanism by which an input buffer works in the presence of ground noise, specifically how capacitance can be used to reduce such noise for a memory input circuit.

Summary of the Invention

[0006] It is therefore an object of the present invention to provide an efficient circuit design technique for an input buffer receiver for a particular memory device**[[,]]** that works to filter ground noise. It is a further object of the invention to provide a means for reducing jitter in an input buffer. This is achieved by attaching a large capacitance to the ~~PMOS~~ bias node of the input buffer receiver.

[0007] These and other objects are achieved by an input buffer receiver comprising: a buffer input portion for receiving an input signal ~~SIGNAL_IN~~;

a large capacitor ~~capacitance CHC~~ between a ~~PMOS~~ bias node and a ~~VSS source~~ lower supply voltage VSS, and a buffer output portion for producing an output signal ~~SIGNAL_OUT1~~. Furthermore, in the input buffer receiver, the ~~VB11 gate~~ biasing voltage of the bias node ~~of transistors P11 and P12~~ is charge coupled to the ~~VSS~~ lower voltage source ~~voltage~~. This results in a quicker response time for the output signal ~~SIGNAL_OUT1~~.

Brief Description of the Drawings

[0008] The foregoing and other objects, aspects, and advantages will be better understood from the following detailed description of a preferred embodiment of the invention, with reference to the drawings, in which:

[0009] FIG. 1 is a diagram of an input buffer receiver according to the prior art.

[0010] FIG. 2 is a diagram of an input buffer receiver according to the present invention.

[0011] FIGS.3A-B show the timing diagrams of the input buffer receiver of the present invention and the definitions of JITTER_RISE and JITTER_FALL.

[0012] FIGS. 4A-B illustrate the workings of ~~capacitance~~ capacitor CHC to reduce JITTER_RISE and JITTER_FALL.

Detailed Description of the Invention

[0013] One embodiment of the present invention is provided below with reference to the accompanying diagrams.

[0014] Referring to FIG. 1, the input buffer receiver of the prior art includes a buffer input portion 100 for receiving an input signal SIGNAL_IN and a buffer output portion 200 for producing an output signal SIGNAL_OUT.

[0015] The buffer input portion 100 is comprised of: NMOS transistors N1 and N2, where a lower supply voltage VSS is applied to the source nodes of NMOS transistors N1 and N2, and PMOS transistors P1 and P2, where an upper voltage supply VDD is applied to the source nodes. The gate nodes of transistors P1 and P2 and the the drains of transistors N1 and P1 are connected together to form the biasing node b1. The biasing voltage VB1 is developed at the biasing node b1 as a result of the configuration of transistors P1 and P2. A parasitic capacitor Cp is present from the biasing node b1 to the ground reference node. ~~and a signal VB1 is applied to the gate nodes of P1 and P2.~~ In the prior art, a reference voltage VREF is applied to the gate of transistor N1, input signal SIGNAL_IN is applied to

the gate of transistor N2~~, and VB1 is applied to the drain of N1 and the drain of P1, as well as the PMOS bias node of P1 and P2~~. Input signal SIGNAL_IN is a low swing signal coming from off chip. The buffer output portion 200 is comprised of a common node for the drain of transistor N2 and drain of transistor P2, which serves as input to inverter I1. The output of inverter I1 is the output signal output SIGNAL_OUT.

[0016] The ground noise (VSS noise), as described above, is developed between the lower supply voltage VSS and the ground reference voltage. The magnitude of the VSS noise affects the delay timing from the input signal SIGNAL_IN to the output signal SIGNAL_OUT. The variation in the delay causes jitter in the rise and fall delays of the buffer and thus slower response times.

[0017] Referring to FIG. 2, the proposed invention is comprised of a similar buffer input portion 101 and a similar buffer output portion 201. The buffer input portion 101 is comprised of: NMOS transistors N11 and N12, where ~~a~~ the lower supply voltage VSS is applied to the source nodes of N11 and N12, and PMOS transistors P11 and P12, where an upper supply voltage VDD is applied to the source nodes. The gate nodes of transistors P11 and P12 and the the drains of transistors N11 and P11 are connected together to form the biasing node b11. The biasing voltage VB11 is

developed at the biasing node b11 as a result of the configuration of transistors P11 and P12. A parasitic capacitor Cp is present from the biasing node b11 to the ground reference node. ~~A signal VB11 is applied to the gate nodes of P11 and P12.~~ A reference supply voltage VREF is applied to the gate of transistor N11, input signal SIGNAL_IN is applied to the gate of N12~~, and VB11 is applied to the drain of N11 and the drain of P11~~. In the present invention, a large ~~capacitance~~ capacitor CHC is attached between the ~~PMOS~~ bias node ~~VB11~~ b11 and the lower supply ~~source~~ voltage VSS. The buffer output portion 201 is comprised of a common node for the drain of transistor N12 and the drain of transistor P12, which serves as input to inverter I11. The output of inverter I11 is the output signal SIGNAL_OUT1 of the invention.

[0018] The large capacitance CHC is in series with the parasitic capacitor Cp ~~capacitance~~ of the input buffer receiver ~~devices~~ transistors N11, P11, and P12. The large capacitor CHC, as connected, is designed to have an extremely large capacitance relative to the parasitic capacitor Cp such that the bias voltage VB11 essentially follows the voltage changes in the lower supply voltage VSS preventing the effects of the VSS noise. This coupling ratio is determined by the formula:

$$\frac{\mathbf{CHC}}{\mathbf{Cp}+\mathbf{CHC}} \approx \mathbf{1}$$

where:

CHC is the capacitance value of the large capacitor CHC.

Cp is the capacitance value of the parasitic capacitor Cp.

[0019] Because of its large coupling ratio (very close to 1), the capacitor CHC essentially charge couples the biasing voltage VB11 ~~gate voltage of the PMOS~~ bias node b11, to the ~~VSS source~~ lower supply voltage VSS, of devices N11 and N12. This forces the transistors N11 and N12 to activate and deactivate essentially simultaneously, allowing for a quicker response time on output signal SIGNAL_OUT1.

[0020] FIGS. 3A-B are diagrams of timed operation showing the input signal SIGNAL_IN, the ~~source~~ lower supply voltage VSS, and the output signal SIGNAL_OUT1 of the proposed invention. It should be noted that the input signal SIGNAL_IN is defined as VIH=VREF+350mv and VIL=VREF-350mv, and VSS is 200mv. The output signal SIGNAL_OUT1 is defined by the ~~delayed signal~~ delay times DELTA1 or DELTA2, when input signal SIGNAL_IN rises, and the delay times DELTA3 or DELTA4, when the input signal SIGNAL_IN falls. The delay time DELTA1 is defined

as the delay from the rising edge of input signal SIGNAL_IN to the rising edge of output signal SIGNAL_OUT, when VSS=200mv. It is the delay on output signal SIGNAL_OUT1 when transistor N12 sees VSS noise and turns on weakly. The delay time DELTA2 is defined as the delay from the rising edge of input signal SIGNAL_IN to the rising edge of output signal SIGNAL_OUT1, when VSS=0v. It is the delay ~~on~~ of the output signal SIGNAL_OUT1 when transistor N12 does not see VSS noise and turns on strongly. The delay time DELTA3 is defined as the delay from the falling edge of input signal SIGNAL_IN to the falling edge of output SIGNAL_OUT1, when VSS=0v. It is the delay ~~on~~ of the input signal SIGNAL_OUT1 when transistor N12 does not see VSS noise and turns off weakly. DELTA4 is defined as the delay from the falling edge of input signal SIGNAL_IN to the falling edge of output signal SIGNAL_OUT1, when VSS=200mv. It is the delay seen on output signal SIGNAL_OUT1 when transistor N12 sees VSS noise and turns off strongly. By definition, the delay times DELTA2 and DELTA4 are smaller than the delay times DELTA1 and DELTA3. The rise time jitter JITTER_RISE is the difference between the delay times DELTA1 and DELTA2 when the input signal SIGNAL_IN rises and the fall time jitter JITTER_FALL is the difference between the delay times DELTA3 and DELTA4 when input signal SIGNAL_IN falls. The intent of the invention ~~capacitance~~ large capacitor

CHC is to reduce rise time jitter JITTER_RISE and fall time jitter JITTER_FALL by primarily having ~~devices~~ transistors P12 and N12, activate, in the presence or absence of ground noise, almost simultaneously.

[0021] FIGS. 4A-B illustrate the workings of large capacitor CHC. In Fig. 4a, the large capacitor is shown in series with the parasitic capacitor Cp. The ~~Its~~ large capacitance coupling ratio of the large capacitor CHC versus the capacitance of the parasitic capacitor Cp creates a charge coupling ~~couples~~ of the ~~PMOS~~ bias node, ~~VB11~~ b11, of the input buffer receiver, to the ~~VSS source~~ lower supply voltage VSS, of the input buffer receiver. This results in a quicker response time for a input signal SIGNAL_OUT1.

[0022] While the invention has been described in terms of the preferred embodiments, those skilled in the art will recognize that various changes in form and details may be made without departing from the spirit and scope of the invention. The present invention covers modifications that fall within the range of the appended claims and their equivalents.

[0023] While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

[0024] What is claimed is:

1. (Amended) An input buffer receiver comprising:

a buffer input portion for receiving an input signal ~~SIGNAL_IN~~, said buffer input portion comprising a bias node;

a large capacitor ~~capacitance~~ between ~~a PMOS~~ the bias node and a ~~VSS source~~ lower supply voltage said large capacitor providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point approaching a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point; and

a buffer output portion in communication with the buffer input portion for producing an output signal ~~SIGNAL_OUT1~~.

2. (Amended) The input buffer receiver of claim 1, wherein the buffer input portion which receives ~~an~~ the input signal ~~SIGNAL_IN~~ further comprises:

a first transistor of a first conductivity type ~~N11~~ having a source node to which ~~a VSS source~~ the lower supply voltage is applied, a gate node to which a reference voltage ~~VREF~~ is applied, and

a drain node at which the biasing voltage is developed ~~to which a signal VB11 is applied~~;

a second transistor of a second conductivity type ~~P11~~ having a drain node which is connected to the drain node of the first transistor ~~N11~~, and a gate node at which the biasing voltage is developed ~~to which a signal VB11 is applied~~, and a source node to which an upper supply voltage source ~~VDD~~ is applied;

a third transistor of the second conductivity type ~~P12~~ having a drain node which is connected to the drain of a fourth transistor ~~N12~~, a gate node at which the biasing voltage is developed ~~to which a signal VB11 is applied~~, and a source node to which ~~an~~ the upper supply voltage source ~~VDD~~ is applied;

a fourth transistor of the first conductivity type ~~N12~~ having a source node to which ~~a VSS source~~ lower suppply voltage is applied, a gate node to which an input signal ~~SIGNAL_IN~~ is applied externally, and a drain node which is ~~the~~ an input to the buffer output portion.

3. (Amended) The input buffer receiver of claim 2 ~~1~~, wherein the first and fourth transistors~~, N11 and N12,~~ are NMOS transistors, and the second and third transistors~~, P11 and P12,~~ are PMOS transistors.

4. (Amended) The input buffer receiver of claim 2 ~~1~~, wherein the large capacitor ~~capacitance~~ is connected between the sources of the first and fourth transistors~~, N11 and N12,~~ of the buffer input portion and the gate of the second transistor ~~P11~~ of the buffer input portion.

5. (Amended) The input buffer receiver of claim 2 ~~1~~, wherein the gate of the second transistor ~~P11~~ is connected to its drain.

6. (Amended) The input buffer receiver of claim 2 ~~1~~, wherein the gate of the second transistor ~~P11~~ is connected to the drain of the first transistor ~~N11~~.

7. (Amended) The input buffer receiver of claim 2 ~~1~~, wherein the gate of the second transistor ~~P11~~ is connected to the gate of the third transistor ~~P12~~.

8. (Amended) The input buffer receiver of claim 2 ~~1~~, wherein the buffer output portion which produces ~~an~~ output signal ~~SIGNAL_OUT1~~ comprises: a first inverter ~~I11~~ connected to the drain of the third transistor ~~P12~~ and the drain of the fourth transistor ~~N12~~;

9. (Amended) The input buffer receiver of claim 2 ~~1~~, wherein ~~P12 and N12~~ the third transistor and the fourth transistor activate almost simultaneously to ~~provide an efficient circuit design technique for filtering~~ minimize the effects of ground noise on a delay jitter factor of said input buffer.

10. (Amended) The input buffer receiver of claim 1, ~~involving a large capacitance coupling ratio, which~~ wherein the large capacitor charge couples the ~~PMOS~~ bias node of the input buffer receiver to the ~~VSS source~~ lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:~~.~~

$$\frac{\mathbf{CHC}}{\mathbf{Cp+CHC}} \approx 1$$

where:

CHC is the capacitance value of the large capacitor, and

Cp is the capacitance value of the parasitic capacitor.

11. (Amended) The input buffer receiver of claim 1, ~~involving a~~ wherein the capacitance value of the large capacitor relative to said parasitic capacitor

~~capacitance coupling ratio, which~~ results in a quicker response time for the output signal ~~a SIGNAL_OUT1~~.

12. (New) An integrated circuit formed on a substrate comprising:

an input buffer receiver for receiving an input signal and connected to said distribution network, said input buffer comprising:

a buffer input portion for receiving the input signal, said buffer input portion comprising a bias node;

a large capacitor between the bias node and a lower supply voltage, said large capacitor providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point approaching a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point ; and

a buffer output portion in communication with the buffer input portion for producing an output signal.

13. (New) The integrated circuit of claim 12, wherein the buffer input portion of the input buffer receiver further comprises:

a first transistor of a first conductivity type having a source node to which the lower supply voltage is applied, a gate node to which a reference voltage is applied, and a drain node at which the biasing voltage is developed ;

a second transistor of a second conductivity type having a drain node which is connected to the drain node of the first transistor, and a gate node at which the biasing voltage is developed, and a source node to which an upper supply voltage source is applied;

a third transistor of the second conductivity type having a drain node which is connected to the drain of a fourth transistor, a gate node at which the biasing voltage is developed, and a source node to which the upper supply voltage source is applied;

a fourth transistor of the first conductivity type having a source node to which lower supply voltage is applied, a gate node to which

an input signal is applied externally, and a drain node which is an input to the buffer output portion.

14. (New) The integrated circuit of claim 13, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

15. (New) The integrated circuit of claim 13, wherein the large capacitor is connected between the sources of the first and fourth transistorsof the buffer input portion and the gate of the second transistor of the buffer input portion.

16. (New) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to its drain.

17. (New) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to the drain of the first transistor.

18. (New) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to the gate of the third transistor.

19. (New) The integrated circuit of claim 13, wherein the buffer output portion which produces output signal comprises: a first inverter connected to the drain of the third transistor and the drain of the fourth transistor;

20. (New) The integrated circuit of claim 13, wherein the third transistor and the fourth transistor activate almost simultaneously to minimize the effects of ground noise on a delay jitter factor of said input buffer.

21. (New) The integrated circuit of claim 12, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{\mathbf{CHC}}{\mathbf{Cp}+\mathbf{CHC}} \approx \mathbf{1}$$

where:

CHC is the capacitance value of the large capacitor, and

Cp is the capacitance value of the parasitic capacitor.

22. (New) The integrated circuit of claim 12, wherein the capacitance value of the large capacitor relative to said parasitic capacitor results in a quicker response time for the output signal.

23. (New) A method for minimizing effects of ground noise on an input buffer receiver comprising the steps of:

forming a buffer input portion for receiving an input signal on a substrate;

forming a bias node within said buffer input portion;

connecting said a lower supply voltage to said buffer input portion;

forming a large capacitor between the bias node and the lower supply voltage said large capacitor providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point approaching a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point; and

forming a buffer output portion on said substrate in communication with the buffer input portion for producing an output signal.

24. (New) The method of claim 23, wherein forming the buffer input portion further comprises the steps of:

forming a first transistor of a first conductivity type on said substrate;

applying the lower supply voltage to a source node of the first transistor;

applying a reference voltage to a gate node of the first transistor;

connecting a drain node of the first transistor to develop as biasing voltage at said drain node;

forming a second transistor of a second conductivity type on said substrate;

connecting a drain node of the second transistor to the drain node of the first transistor;

connecting a gate node of the second transistor to the drain node of the first transistor for developing the biasing voltage; and

connecting a source node of the second transistor to an upper supply voltage;

forming a third transistor of the second conductivity type on said substrate;

connecting a drain node of the third transistor to the drain of a fourth transistor;

connecting a gate node of the third transistor to the drain node of the first transistor for developing the biasing voltage;

connecting a source node of the third transistor to the upper supply voltage source;

forming a fourth transistor of the first conductivity type on said substrate;

connecting a source node of the fourth transistor to the lower supply voltage;

connecting a gate node of the fourth transistor to receive an input signal externally; and

connecting a drain node of the fourth transistor to an input to the buffer output portion.

25. (New) The method of claim 24, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

26. (New) The method of claim 24, wherein forming the large capacitor comprises the step of:

connecting said large capacitor between the sources of the first and fourth transistors of the buffer input portion and the gate of the second transistor of the buffer input portion.

27. (New) The method of claim 24, wherein forming the buffer input portion further comprises the steps of:

connecting the gate of the second transistor to its drain.

28. (New) The method of claim 24, wherein forming the buffer input portion further comprises the steps of:

connecting the gate of the second transistor to the gate of the third transistor.

29. (New) The method of claim 24, wherein forming the buffer output portion which produces output signal comprises the step of:

forming a first inverter on said substrate; and

connecting an input of said first inverter to the drain of the third transistor and the drain of the fourth transistor;

30. (New) The method of claim 24, wherein the third transistor and the fourth transistor activate almost simultaneously to minimize the effects of ground noise on a delay jitter factor of said input buffer.

31. (New) The method of claim 23, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{\mathbf{CHC}}{\mathbf{Cp}+\mathbf{CHC}} \approx \mathbf{1}$$

where:

CHC is the capacitance value of the large capacitor, and

Cp is the capacitance value of the parasitic capacitor.

32. (New) The method of claim 23, wherein the capacitance value of the large capacitor relative to said parasitic capacitor results in a quicker response time for the output signal.

33. (New) An apparatus for minimizing effects of ground noise on an input buffer receiver comprising:

means for forming a buffer input portion for receiving an input signal on a substrate;

means for forming a bias node within said buffer input portion;

means for connecting said a lower supply voltage to said buffer input portion;

means for forming a large capacitor between the bias node and the lower supply voltage said large capacitor providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point approaching a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point; and

means for forming a buffer output portion on said substrate in communication with the buffer input portion for producing an output signal.

34. (New) The apparatus of claim 23, wherein forming the buffer input portion further comprises:

means for forming a first transistor of a first conductivity type on said substrate;

means for applying the lower supply voltage to a source node of the first transistor;

means for applying a reference voltage to a gate node of the first transistor;

means for connecting a drain node of the first transistor to develop as biasing voltage at said drain node;

means for forming a second transistor of a second conductivity type on said substrate;

means for connecting a drain node of the second transistor to the drain node of the first transistor;

means for connecting a gate node of the second transistor to the drain node of the first transistor for developing the biasing voltage; and

means for connecting a source node of the second transistor to an upper supply voltage;

means for forming a third transistor of the second conductivity type on said substrate;

means for connecting a drain node of the third transistor to the drain of a fourth transistor;

means for connecting a gate node of the third transistor to the drain node of the first transistor for developing the biasing voltage;

means for connecting a source node of the third transistor to the upper supply voltage source;

means for forming a fourth transistor of the first conductivity type on said substrate;

means for connecting a source node of the fourth transistor to the lower supply voltage;

means for connecting a gate node of the fourth transistor to receive an input signal externally; and

connecting a drain node of the fourth transistor to an input to the buffer output portion.

35. (New) The apparatus of claim 24, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

36. (New) The apparatus of claim 24, wherein means for forming the large capacitor comprises:

means for connecting said large capacitor between the sources of the first and fourth transistors of the buffer input portion and the gate of the second transistor of the buffer input portion.

37. (New) The apparatus of claim 24, wherein means for forming the buffer input portion further comprises:

means for connecting the gate of the second transistor to its drain.

38. (New) The apparatus of claim 24, wherein means for forming the buffer input portion further comprises the steps of:

means for connecting the gate of the second transistor to the gate of the third transistor.

39. (New) The apparatus of claim 24, wherein means for forming the buffer output portion which produces output signal comprises:

means for forming a first inverter on said substrate; and

means for connecting an input of said first inverter to the drain of the third transistor and the drain of the fourth transistor;

40. (New) The apparatus of claim 24, wherein the third transistor and the fourth transistor activate almost simultaneously to minimize the effects of ground noise on a delay jitter factor of said input buffer.

41. (New) The apparatus of claim 23, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{\mathbf{CHC}}{\mathbf{Cp} + \mathbf{CHC}} \approx \mathbf{1}$$

where:

CHC is the capacitance value of the large capacitor CHC, and

Cp is the capacitance value of the parasitic capacitor Cp.

42. (New) The apparatus of claim 23, wherein the capacitance value of the large capacitor relative to said parasitic capacitor results in a quicker response time for the output signal.

Abstract

[0025] A particular input buffer receiver includes a buffer input portion for receiving an input signal ~~SIGNAL_IN~~, a large capacitor ~~capacitance CHC~~ between ~~the PMOS~~ a bias node and the ~~VSS source~~ lower supply voltage, and a buffer output portion for producing an output signal ~~SIGNAL_OUT1~~. The circuit works to remove ground noise by charge coupling the ~~VB11~~ bias voltage developed at the bias node to the ~~VSS source~~ lower supply voltage of the input device.

Clean Copy of Specification showing changes

LOW JITTER INPUT BUFFER WITH SMALL INPUT SIGNAL SWING

Background of the Invention

Field of the Invention

[0001] The present invention generally relates to an interface circuit, and particularly to a low jitter input buffer.

Description of Related Art

[0002] Major design efforts have been directed at circuit design techniques involving input circuits for memory devices. A number of solutions have been proposed.

[0003] U.S. Patent 5,978,310 (Bae et al) describes an input buffer for a DRAM memory device, which removes noise from the row address strobe. The device has a data output enable, which can be delayed for a predetermined time, and which also produces a control signal for the output. There is also a buffer output for producing the noise free input according to the control signal.

[0004] U.S. Patent 6,002,618 (Komarek et al) discloses an NMOS input receiver circuit for a read only memory. It includes a feedback loop to control hysteresis. There is a second stage and an additional output for the receiver. Switching noise from inside the memory is isolated and cannot be fed back into the receiver circuit to affect the TTL voltage levels. Wide, long FET sizes are used to minimize manufacture variations in the receiver switching levels.

[0005] What is still needed is a mechanism by which an input buffer works in the presence of ground noise, specifically how capacitance can be used to reduce such noise for a memory input circuit.

Summary of the Invention

[0006] It is therefore an object of the present invention to provide an efficient circuit design technique for an input buffer receiver for a particular memory device that works to filter ground noise. It is a further object of the invention to provide a means for reducing jitter in an input buffer. This is achieved by attaching a large capacitance to the bias node of the input buffer receiver.

[0007] These and other objects are achieved by an input buffer receiver comprising: a buffer input portion for receiving an input signal; a large capacitor between a bias node and a lower supply voltage VSS, and a

buffer output portion for producing an output signal. Furthermore, in the input buffer receiver, the biasing voltage of the bias node is charge coupled to the lower voltage source. This results in a quicker response time for the output signal.

Brief Description of the Drawings

[0008] The foregoing and other objects, aspects, and advantages will be better understood from the following detailed description of a preferred embodiment of the invention, with reference to the drawings, in which:

[0009] FIG. 1 is a diagram of an input buffer receiver according to the prior art.

[0010] FIG. 2 is a diagram of an input buffer receiver according to the present invention.

[0011] FIGS.3A-B show the timing diagrams of the input buffer receiver of the present invention and the definitions of JITTER_RISE and JITTER_FALL.

[0012] FIGS. 4A-B illustrate the workings of capacitor CHC to reduce JITTER_RISE and JITTER_FALL.

Detailed Description of the Invention

[0013] One embodiment of the present invention is provided below with reference to the accompanying diagrams.

[0014] Referring to FIG. 1, the input buffer receiver of the prior art includes a buffer input portion 100 for receiving an input signal SIGNAL_IN and a buffer output portion 200 for producing an output signal SIGNAL_OUT.

[0015] The buffer input portion 100 is comprised of: NMOS transistors N1 and N2, where a lower supply voltage VSS is applied to the source nodes of NMOS transistors N1 and N2, and PMOS transistors P1 and P2, where an upper voltage supply VDD is applied to the source nodes. The gate nodes of transistors P1 and P2 and the the drains of transistors N1 and P1 are connected together to form the biasing node b1. The biasing voltage VB1 is developed at the biasing node b1 as a result of the configuration of transistors P1 and P2. A parasitic capacitor Cp is present from the biasing node b1 to the ground reference node. In the prior art, a reference voltage VREF is applied to the gate of transistor N1, input signal SIGNAL_IN is applied to the gate of transistor N2. Input signal SIGNAL_IN is a low swing signal coming from off chip. The buffer output portion 200 is comprised of a common node for the drain of transistor N2 and drain of transistor P2,

which serves as input to inverter I1. The output of inverter I1 is the output signal output SIGNAL_OUT.

[0016] The ground noise (VSS noise), as described above, is developed between the lower supply voltage VSS and the ground reference voltage. The magnitude of the VSS noise affects the delay timing from the input signal SIGNAL_IN to the output signal SIGNAL_OUT. The variation in the delay causes jitter in the rise and fall delays of the buffer and thus slower response times.

[0017] Referring to FIG. 2, the proposed invention is comprised of a similar buffer input portion 101 and a similar buffer output portion 201. The buffer input portion 101 is comprised of: NMOS transistors N11 and N12, where the lower supply voltage VSS is applied to the source nodes of N11 and N12, and PMOS transistors P11 and P12, where an upper supply voltage VDD is applied to the source nodes. The gate nodes of transistors P11 and P12 and the the drains of transistors N11 and P11 are connected together to form the biasing node b11. The biasing voltage VB11 is developed at the biasing node b11 as a result of the configuration of transistors P11 and P12. A parasitic capacitor Cp is present from the biasing node b11 to the ground reference node. A reference supply voltage VREF is applied to the gate of transistor N11, input signal SIGNAL_IN is applied to the gate of N12. In the present invention, a large

capacitor CHC is attached between the bias node b11 and the lower supply voltage VSS. The buffer output portion 201 is comprised of a common node for the drain of transistor N12 and the drain of transistor P12, which serves as input to inverter I11. The output of inverter I11 is the output signal SIGNAL_OUT1 of the invention.

[0018] The large capacitance CHC is in series with the parasitic capacitor Cp of the input buffer receiver transistors N11, P11, and P12. The large capacitor CHC, as connected, is designed to have an extremely large capacitance relative to the parasitic capacitor Cp such that the bias voltage VB11 essentially follows the voltage changes in the lower supply voltage VSS preventing the effects of the VSS noise. This coupling ratio is determined by the formula:

$$\frac{\mathbf{CHC}}{\mathbf{Cp}+\mathbf{CHC}} \approx \mathbf{1}$$

where:

CHC is the capacitance value of the large capacitor CHC.

Cp is the capacitance value of the parasitic capacitor Cp.

[0019] Because of its large coupling ratio (very close to 1), the capacitor CHC essentially charge couples the biasing voltage VB11 bias node b11, to the lower supply voltage VSS, of devices N11 and N12. This forces the transistors N11 and N12 to activate and deactivate essentially simultaneously, allowing for a quicker response time on output signal SIGNAL_OUT1.

[0020] FIGS. 3A-B are diagrams of timed operation showing the input signal SIGNAL_IN, the lower supply voltage VSS, and the output signal SIGNAL_OUT1 of the proposed invention. It should be noted that the input signal SIGNAL_IN is defined as VIH=VREF+350mv and VIL=VREF-350mv, and VSS is 200mv. The output signal SIGNAL_OUT1 is defined by the delay times DELTA1 or DELTA2, when input signal SIGNAL_IN rises, and the delay times DELTA3 or DELTA4, when the input signal SIGNAL_IN falls. The delay time DELTA1 is defined as the delay from the rising edge of input signal SIGNAL_IN to the rising edge of output signal SIGNAL_OUT, when VSS=200mv. It is the delay on output signal SIGNAL_OUT1 when transistor N12 sees VSS noise and turns on weakly. The delay time DELTA2 is defined as the delay from the rising edge of input signal SIGNAL_IN to the rising edge of output signal SIGNAL_OUT1, when VSS=0v. It is the delay of the output signal SIGNAL_OUT1 when transistor N12 does not see VSS noise and turns on

strongly. The delay time DELTA3 is defined as the delay from the falling edge of input signal SIGNAL_IN to the falling edge of output SIGNAL_OUT1, when VSS=0v. It is the delay of the input signal SIGNAL_OUT1 when transistor N12 does not see VSS noise and turns off weakly. DELTA4 is defined as the delay from the falling edge of input signal SIGNAL_IN to the falling edge of output signal SIGNAL_OUT1, when VSS=200mv. It is the delay seen on output signal SIGNAL_OUT1 when transistor N12 sees VSS noise and turns off strongly. By definition, the delay times DELTA2 and DELTA4 are smaller than the delay times DELTA1 and DELTA3. The rise time jitter JITTER_RISE is the difference between the delay times DELTA1 and DELTA2 when the input signal SIGNAL_IN rises and the fall time jitter JITTER_FALL is the difference between the delay times DELTA3 and DELTA4 when input signal SIGNAL_IN falls. The intent of the invention large capacitor CHC is to reduce rise time jitter JITTER_RISE and fall time jitter JITTER_FALL by primarily having transistors P12 and N12, activate, in the presence or absence of ground noise, almost simultaneously.

[0021] FIGS. 4A-B illustrate the workings of large capacitor CHC. In Fig. 4a, the large capacitor is shown in series with the parasitic capacitor Cp. The large capacitance coupling ratio of the large capacitor CHC versus the capacitance of the parasitic capacitor Cp creates a charge coupling of

the bias node, b11, of the input buffer receiver, to the lower supply voltage VSS, of the input buffer receiver. This results in a quicker response time for a input signal SIGNAL_OUT1.

[0022] While the invention has been described in terms of the preferred embodiments, those skilled in the art will recognize that various changes in form and details may be made without departing from the spirit and scope of the invention. The present invention covers modifications that fall within the range of the appended claims and their equivalents.

[0023] While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

[0024] What is claimed is:

1. (Amended) An input buffer receiver comprising:

a buffer input portion for receiving an input signal, said buffer input portion comprising a bias node;

a large capacitor between the bias node and a lower supply voltage said large capacitor providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point approaching a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point; and

a buffer output portion in communication with the buffer input portion for producing an output signal.

2. (Amended) The input buffer receiver of claim 1, wherein the buffer input portion which receives the input signal further comprises:

a first transistor of a first conductivity type having a source node to which the lower supply voltage is applied, a gate node to which a reference voltage is applied, and a drain node at which the biasing voltage is developed ;

a second transistor of a second conductivity type having a drain node which is connected to the drain node of the first transistor, and a gate node at which the biasing voltage is developed, and a source node to which an upper supply voltage source is applied;

a third transistor of the second conductivity type having a drain node which is connected to the drain of a fourth transistor, a gate node at which the biasing voltage is developed, and a source node to which the upper supply voltage source is applied;

a fourth transistor of the first conductivity type having a source node to which lower suppply voltage is applied, a gate node to which an input signal is applied externally, and a drain node which is an input to the buffer output portion.

3. (Amended) The input buffer receiver of claim 2, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

4. (Amended) The input buffer receiver of claim 2, wherein the large capacitor is connected between the sources of the first and fourth

transistorsof the buffer input portion and the gate of the second transistor of the buffer input portion.

5. (Amended) The input buffer receiver of claim 2, wherein the gate of the second transistor is connected to its drain.

6. (Amended) The input buffer receiver of claim 2, wherein the gate of the second transistor is connected to the drain of the first transistor.

7. (Amended) The input buffer receiver of claim 2, wherein the gate of the second transistor is connected to the gate of the third transistor.

8. (Amended) The input buffer receiver of claim 2, wherein the buffer output portion which produces output signal comprises: a first inverter connected to the drain of the third transistor and the drain of the fourth transistor;

9. (Amended) The input buffer receiver of claim 2, wherein the third transistor and the fourth transistor activate almost simultaneously to minimize the effects of ground noise on a delay jitter factor of said input buffer.

10. (Amended) The input buffer receiver of claim 1, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

where:

CHC is the capacitance value of the large capacitor, and

Cp is the capacitance value of the parasitic capacitor.

11. (Amended) The input buffer receiver of claim 1, wherein the capacitance value of the large capacitor relative to said parasitic capacitor results in a quicker response time for the output signal.

12. (New) An integrated circuit formed on a substrate comprising:

an input buffer receiver for receiving an input signal and connected to said distribution network, said input buffer comprising:

a buffer input portion for receiving the input signal, said buffer input portion comprising a bias node;

a large capacitor between the bias node and a lower supply voltage, said large capacitor providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node

and a ground reference point approaching a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point ; and

a buffer output portion in communication with the buffer input portion for producing an output signal.

13. (New) The integrated circuit of claim 12, wherein the buffer input portion of the input buffer receiver further comprises:

a first transistor of a first conductivity type having a source node to which the lower supply voltage is applied, a gate node to which a reference voltage is applied, and a drain node at which the biasing voltage is developed ;

a second transistor of a second conductivity type having a drain node which is connected to the drain node of the first transistor, and a gate node at which the biasing voltage is developed, and a source node to which an upper supply voltage source is applied;

a third transistor of the second conductivity type having a drain node which is connected to the drain of a fourth transistor, a gate node at which the biasing voltage is developed, and a source node to which the upper supply voltage source is applied;

a fourth transistor of the first conductivity type having a source node to which lower supply voltage is applied, a gate node to which an input signal is applied externally, and a drain node which is an input to the buffer output portion.

14. (New) The integrated circuit of claim 13, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

15. (New) The integrated circuit of claim 13, wherein the large capacitor is connected between the sources of the first and fourth transistorsof the buffer input portion and the gate of the second transistor of the buffer input portion.

16. (New) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to its drain.

17. (New) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to the drain of the first transistor.

18. (New) The integrated circuit of claim 13, wherein the gate of the second transistor is connected to the gate of the third transistor.

19. (New) The integrated circuit of claim 13, wherein the buffer output portion which produces output signal comprises: a first inverter connected to the drain of the third transistor and the drain of the fourth transistor;

20. (New) The integrated circuit of claim 13, wherein the third transistor and the fourth transistor activate almost simultaneously to minimize the effects of ground noise on a delay jitter factor of said input buffer.

21. (New) The integrated circuit of claim 12, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

where:-

CHC is the capacitance value of the large capacitor, and

Cp is the capacitance value of the parasitic capacitor.

22. (New) The integrated circuit of claim 12, wherein the capacitance value of the large capacitor relative to said parasitic capacitor results in a quicker response time for the output signal.

23. (New) A method for minimizing effects of ground noise on an input buffer receiver comprising the steps of:

forming a buffer input portion for receiving an input signal on a substrate;

forming a bias node within said buffer input portion;

connecting said a lower supply voltage to said buffer input portion;

forming a large capacitor between the bias node and the lower supply voltage said large capacitor providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point approaching a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize

effects of a ground noise signal between the lower supply voltage and the ground reference point; and

forming a buffer output portion on said substrate in communication with the buffer input portion for producing an output signal.

24. (New) The method of claim 23, wherein forming the buffer input portion further comprises the steps of:

forming a first transistor of a first conductivity type on said substrate;

applying the lower supply voltage to a source node of the first transistor;

applying a reference voltage to a gate node of the first transistor;

connecting a drain node of the first transistor to develop as biasing voltage at said drain node;

forming a second transistor of a second conductivity type on said substrate;

connecting a drain node of the second transistor to the drain node of the first transistor;

connecting a gate node of the second transistor to the drain node of the first transistor for developing the biasing voltage; and

connecting a source node of the second transistor to an upper supply voltage;

forming a third transistor of the second conductivity type on said substrate;

connecting a drain node of the third transistor to the drain of a fourth transistor;

connecting a gate node of the third transistor to the drain node of the first transistor for developing the biasing voltage;

connecting a source node of the third transistor to the upper supply voltage source;

forming a fourth transistor of the first conductivity type on said substrate;

connecting a source node of the fourth transistor to the lower supply voltage;

connecting a gate node of the fourth transistor to receive an input signal externally; and

connecting a drain node of the fourth transistor to an input to the buffer output portion.

25. (New) The method of claim 24, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

26. (New) The method of claim 24, wherein forming the large capacitor comprises the step of:

connecting said large capacitor between the sources of the first and fourth transistors of the buffer input portion and the gate of the second transistor of the buffer input portion.

27. (New) The method of claim 24, wherein forming the buffer input portion further comprises the steps of:

connecting the gate of the second transistor to its drain.

28. (New) The method of claim 24, wherein forming the buffer input portion further comprises the steps of:

connecting the gate of the second transistor to the gate of the third transistor.

29. (New) The method of claim 24, wherein forming the buffer output portion which produces output signal comprises the step of:

forming a first inverter on said substrate; and

connecting an input of said first inverter to the drain of the third transistor and the drain of the fourth transistor;

30. (New) The method of claim 24, wherein the third transistor and the fourth transistor activate almost simultaneously to minimize the effects of ground noise on a delay jitter factor of said input buffer.

31. (New) The method of claim 23, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{\mathbf{CHC}}{\mathbf{Cp} + \mathbf{CHC}} \approx \mathbf{1}$$

where:

CHC is the capacitance value of the large capacitor, and

Cp is the capacitance value of the parasitic capacitor.

32. (New) The method of claim 23, wherein the capacitance value of the large capacitor relative to said parasitic capacitor results in a quicker response time for the output signal.

33. (New) An apparatus for minimizing effects of ground noise on an input buffer receiver comprising:

means for forming a buffer input portion for receiving an input signal on a substrate;

means for forming a bias node within said buffer input portion;

means for connecting said a lower supply voltage to said buffer input portion;

means for forming a large capacitor between the bias node and the lower supply voltage said large capacitor providing a coupling ratio between said large capacitor and a parasitic capacitor coupled between said bias node and a ground reference point approaching a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of a ground noise signal between the lower supply voltage and the ground reference point; and

means for forming a buffer output portion on said substrate in communication with the buffer input portion for producing an output signal.

34. (New) The apparatus of claim 23, wherein forming the buffer input portion further comprises:

means for forming a first transistor of a first conductivity type on said substrate;

means for applying the lower supply voltage to a source node of the first transistor;

means for applying a reference voltage to a gate node of the first transistor;

means for connecting a drain node of the first transistor to develop as biasing voltage at said drain node;

means for forming a second transistor of a second conductivity type on said substrate;

means for connecting a drain node of the second transistor to the drain node of the first transistor;

means for connecting a gate node of the second transistor to the drain node of the first transistor for developing the biasing voltage; and

means for connecting a source node of the second transistor to an upper supply voltage;

means for forming a third transistor of the second conductivity type on said substrate;

means for connecting a drain node of the third transistor to the drain of a fourth transistor;

means for connecting a gate node of the third transistor to the drain node of the first transistor for developing the biasing voltage;

means for connecting a source node of the third transistor to the upper supply voltage source;

means for forming a fourth transistor of the first conductivity type on said substrate;

means for connecting a source node of the fourth transistor to the lower supply voltage;

means for connecting a gate node of the fourth transistor to receive an input signal externally; and

connecting a drain node of the fourth transistor to an input to the buffer output portion.

35. (New) The apparatus of claim 24, wherein the first and fourth transistors are NMOS transistors, and the second and third transistors are PMOS transistors.

36. (New) The apparatus of claim 24, wherein means for forming the large capacitor comprises:

means for connecting said large capacitor between the sources of the first and fourth transistors of the buffer input portion and the gate of the second transistor of the buffer input portion.

37. (New) The apparatus of claim 24, wherein means for forming the buffer input portion further comprises:

means for connecting the gate of the second transistor to its drain.

38. (New) The apparatus of claim 24, wherein means for forming the buffer input portion further comprises the steps of:

means for connecting the gate of the second transistor to the gate of the third transistor.

39. (New) The apparatus of claim 24, wherein means for forming the buffer output portion which produces output signal comprises:

means for forming a first inverter on said substrate; and

means for connecting an input of said first inverter to the drain of the third transistor and the drain of the fourth transistor;

40. (New) The apparatus of claim 24, wherein the third transistor and the fourth transistor activate almost simultaneously to minimize the effects of ground noise on a delay jitter factor of said input buffer.

41. (New) The apparatus of claim 23, wherein the large capacitor charge couples the bias node of the input buffer receiver to the lower supply voltage of the input buffer receiver and wherein a capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

where:

CHC is the capacitance value of the large capacitor CHC, and

Cp is the capacitance value of the parasitic capacitor Cp.

42. (New) The apparatus of claim 23, wherein the capacitance value of the large capacitor relative to said parasitic capacitor results in a quicker response time for the output signal.

Abstract

[0025] A particular input buffer receiver includes a buffer input portion for receiving an input signal, a large capacitor between a bias node and the lower supply voltage, and a buffer output portion for producing an output signal. The circuit works to remove ground noise by charge coupling the bias voltage developed at the bias node to the lower supply voltage of the input device.

Annotated Drawing Sheet(s) Showing Changes

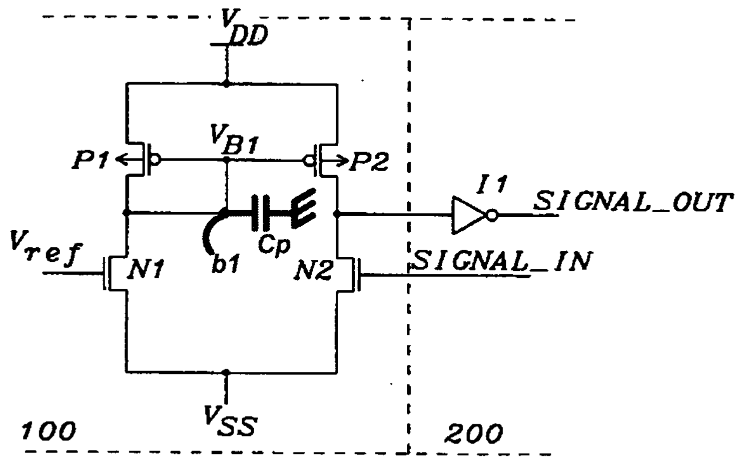

FIG. 1 - Prior Art

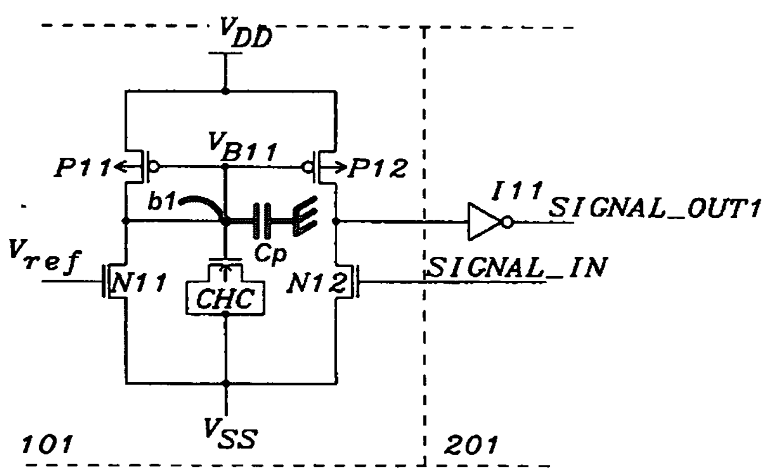

FIG. 2

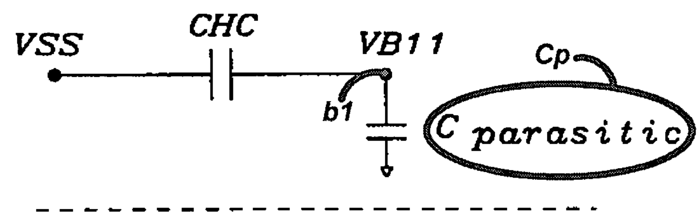
VSS
CHC
VB11
Cp
b1
C parasitic

FIG. 4A

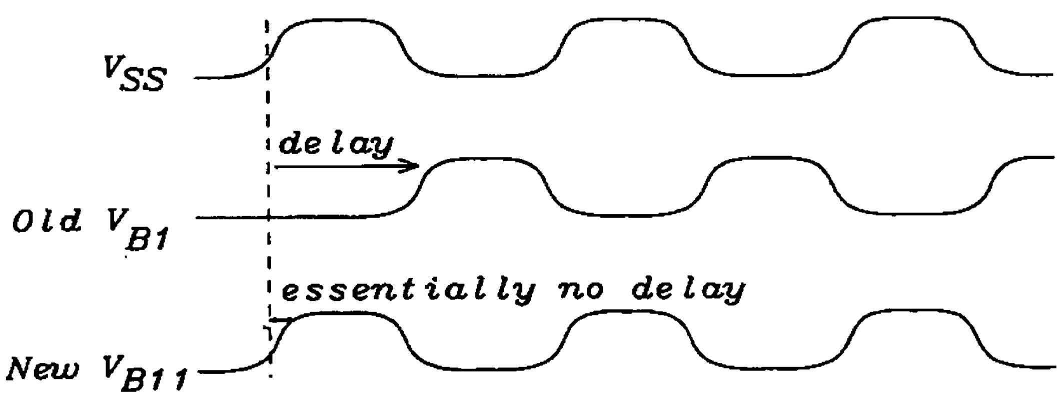
V_{SS}
delay
Old V_{B1}
essentially no delay
New V_{B11}

FIG. 4B

Drawing Replacement Drawing Sheet(s)